



PATENT

IN THE UNITED STATES PATENT OFFICE

Applicant: Richard P. Burnley  
Assignee: Xilinx, Inc.  
Title: "Timing Performance Analysis"

Serial No.: 10/084,515      File Date: February 27, 2002  
Examiner: Andrea Liu      Art Unit: 2825  
Docket No.: X-1081 US      Conf. No.: 7721

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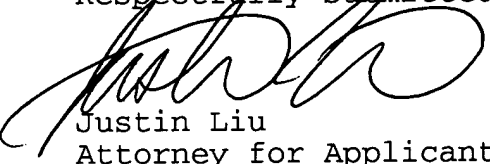
Dear Sir:

Pursuant to 37 C.F.R. 1.56, Applicant brings to the attention of the Examiner the One Hundred Two (102) references listed in the attached Form PTO-1449. A copy of each is enclosed herein.

These references were cited in related U.S. patent applications. The enclosed references are being cited after the receipt of a first office action but prior to any final action.

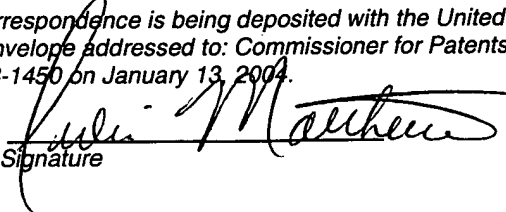
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Respectfully submitted,

  
Justin Liu  
Attorney for Applicant  
Reg. No. 51,959

I hereby certify that this correspondence is being deposited with the United States Postal Service as **first class mail** in an envelope addressed to: Commissioner for Patents, P.O. BOX 1450, Alexandria, Virginia, 22313-1450 on January 13, 2004.

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Substitute for form 1449A/PTO		<b>Complete if Known</b>	
		Applicant / Conf. No.	10/084,515 / 7221
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)		Filing Date	February 27, 2002
		First Named Inventor	Richard P. Burnley
		Art Unit	2825
		Examiner Name	Andrea Liu
		Attorney Docket Number	X-1081 US
Sheet	2	of	7

OTHER – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		SAYFE KIAEI et al., "VLSI DESIGN OF DYNAMICALLY RECONFIGURABLE ARRAY PROCESSOR-DRAP," IEEE, February 1989, pp. 2484-2488, V3.6, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		VASON P. SRINIVASA, "FIELD PROGRAMMABLE GATE ARRAY (FPGA) IMPLEMENTATION OF DIGITAL SYSTEMS: AN ALTERNATIVE TO ASIC," IEEE, May 1991, pp. 309-314, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		G. MAKI et al., "A RECONFIGURABLE DATA PATH PROCESSOR," IEEE, August 1991, pp. 18-4.1 to 18-4.4, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		JACOB DAVIDSON, "FPGA IMPLEMENTATION OF RECONFIGURABLE MICROPROCESSOR," IEEE, March 1993, pp. 3.2.1 - 3.2.4, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		CHRISTIAN ISELI et al., "BEYOND SUPERSCALER USING FPGA's," IEEE, April 1993, pp. 486-490, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
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		WILLIAM S. CARTER, "THE FUTURE OF PROGRAMMABLE LOGIC and ITS IMPACT ON DIGITAL SYSTEM DESIGN," April 1994, IEEE, pp. 10-16, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
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		OSAMA T. ALBAHARNA, "AREA & TIME LIMITATIONS OF FPGA-BASED VIRTUAL HARDWARE," IEEE, April 1994, pp. 184 - 189, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	

Examiner Signature		Date Considered	
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Sheet	4	of	7	Attorney Docket Number	X-1081 US

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		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, pp 2-109 to 2-117, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
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		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 1994, Revised 1995, pp 2-107 to 2-108, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
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		YAMIN LI et al., "AIZUP-A PIPELINED PROCESSOR DESIGN & IMPLEMENTATION ON XILINX FPGA CHIP," IEEE, September 1996, pp 98-106, 98-106, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		RALPH D. WITTIG et al., "ONECHIP: AN FPGA PROCESSOR WITH RECONFIGURABLE LOGIC, April 17, 1996, pp 126-135, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
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		WILLIAM B. ANDREW et al., "A FIELD PROGRAMMABLE SYSTEM CHIP WHICH COMBINES FPGA & ASIC CIRCUITRY," IEEE, May 16, 1999, pp. 183-186, IEEE, 3 Park Avenue, 17th Floor, New York, NY 10016-5997	
		XILINX, INC., "THE PROGRAMMABLE LOGIC DATA BOOK," 2000, Ch. 3 pp 3-1 TO 3-117, Xilinx, Inc., 2100 Logic Drive, San Jose, CA 95124	

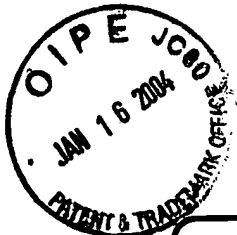
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		<b>Art Unit</b>	2825		
		<b>Examiner Name</b>	Andrea Liu		
<b>Sheet</b>	6	<b>of</b>	7	<b>Attorney Docket Number</b>	X-1081 US

<b>OTHER -- NON PATENT LITERATURE DOCUMENTS</b>			
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		<u>XILINX, INC.</u> , "THE PROGRAMMABLE LOGIC DATA BOOK," 2000, Ch 3, pp 3-7 TO 3-17; 3-76 TO 3-87, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	
		INTERNATIONAL BUSINESS MACHINES, "PROCESSOR LOCAL BUS" Architecture Specifications, 32-Bit Implementation, April 2000, First Edition, V2.9, pp. 1-76, IBM Corporation, Department H83A, P.O. Box 12195, Research Triangle Park, NC 27709	
		<u>XILINX, INC.</u> , "VIRTEX II PLATFORM FPGA HANDBOOK, December 6, 2000, v1.1, pp 33-75, Xilinx, Inc., 2100 Logic Drive, San Jose, CA. 95124.	

<b>Examiner Signature</b>		<b>Date Considered</b>	
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